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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/633,297 | 08/03/2000 | Arron Uri Levy | DENSE-015X | 2376 |

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| EXAMINER | |
|---|---|
| GRAYBILL, DAVID E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/633,297 | LEVY ET AL. | |
| | Examiner | Art Unit | |
| | David E. Graybill | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The amendment filed 8-2-5 proposes amendments to the claims that do not comply with 37 CFR 1.173(b), which sets forth the manner of making amendments in reissue applications. Specifically, new claims 7-14 are not completely underlined. A supplemental paper correctly amending the reissue application is required.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sugano (JP60200559).

In the English abstract and Figures, Sugano discloses a chip stack comprising: at least two packaged chips 2, 24, each of the packaged chips having opposite sides and a multiplicity of leads 5, 27 extending from each of the opposite sides thereof; and at least one frame 30 extending along at least each of the opposite sides of the packaged chips and comprising: an upper surface having only first and second rows of conductive pads 32, 33 disposed thereon, each of the first and second rows of conductive pads

extending along a respective one of the opposite sides of the packaged chips; and a lower surface having only third and fourth rows of conductive pads 36, 37 disposed thereon, each of the third and fourth rows of conductive pads extending along a respective one of the opposite sides of the packaged chips; each of the leads of one of the packaged chips 2 being electrically connected to a respective one of the conductive pads of the first and second rows disposed on the upper surface of the frame, with each of the leads of one of the packaged chips 2 being electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame; wherein the packaged chips each comprise a TSOP packaged chip; wherein each of the conductive pads of the first and second rows disposed on the upper surface of the frame is electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

Claims 10-14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sugano (5028986).

At column 5, line 32 to column 7, line 30, Sugano discloses the following:

A chip stack comprising: two or more packaged chips arranged in a stack one 1b above the other 1a, each of the packaged chips having a first side, a second side opposite the first side, and a multiplicity of leads 3a, 3b

extending from each of the first side and the second side; at least one framing structure 9b having a first side frame portion extending along the first side of a selected one 1b of the two or more packaged chips, a second side frame portion extending along the second side of the selected one, and two end frame portions, the first and second side frame portions and the end frame portions forming an aperture "through opening," a selected first one 1b of the two or more packaged chips disposed at least partially in the aperture, the first side frame portion having an upper surface with a first row of conductive pads 11b disposed therealong, and a lower surface with a second row of conductive pads 10b disposed therealong, the second side frame portion having an upper surface with a third row of conductive pads 11b disposed therealong, and a lower surface with a fourth row of conductive pads 10b disposed therealong; each of the leads 3b of one of the packaged chips 1b being electrically connected to a respective one of the conductive pads of the first and third rows of conductive pads, with each of the leads of the other of the packaged chips 1a being electrically connected to a respective one of the conductive pads of the second and fourth rows of conductive pads; at least one of the conductive pads of the first row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads, and at least one of the conductive pads of the third row of conductive pads is electrically

connected to a respective one of the conductive pads of the second row of conductive pads; the aperture has inner walls facing the selected first one of the two or more packaged chips, the inner walls being separated, by a gap (illustrated in the drawings, not labeled), from the packaged chip along at least one side of the package chip.

A chip stack comprising: two or more packaged chips arranged in a stack one above the other, each of the packaged chips having a first side, a second side opposite the first side, and a multiplicity of leads extending from each of the first side and the second side; a first side frame portion extending along the first side of a selected one of the two or more packaged chips, a second side frame portion extending along the second side of the selected one, the first side frame portion having an upper surface with a first row of conductive pads disposed therealong, and a lower surface with a second row of conductive pads disposed therealong, the second side frame portion having an upper surface with a third row of conductive pads disposed therealong, and a lower surface with a fourth row of conductive pads disposed therealong; each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the first and third rows of conductive pads, with each of the leads of the other of the packaged chips being electrically connected to a respective one of the conductive pads of the second and fourth rows of conductive pads; at least

one of the conductive pads of the first row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads, and at least one of the conductive pads of the third row of conductive pads is electrically connected to a respective one of the conductive pads of the second row of conductive pads.

Applicant's amendment and remarks filed 8-2-5 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant contends that Sugano (JP60200559) does not disclose a frame.

This contention is respectfully traversed because, as applied to the rejection, Sugano discloses a frame 30, at least because Sugano inherently discloses the constructional system 30 that gives shape or strength, and an open structure 30 made for supporting the chips.

Also, applicant asserts, "the Sugano substrate does not extend along the sides of the packaged chips."

This assertion is respectfully traversed because, as cited, Sugano at least discloses at least one frame 30 extending in a line parallel with the length or direction of at least each of the opposite sides of the packaged chips.

Claims 1-6 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art does not teach the claimed invention as a whole, including the steps of cutting.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**For information on the status of this application applicant should check PAIR:** Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.**

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
18-Oct-05